REMARKS

Claims 1, 3-6 and 8-18 are pending in the present application. Claims 1 and 18 have been amended. Claims 2 and 7 have been canceled.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Drawings

The drawings have been objected to as failing to comply with 37 C.F.R. 1.84(p)(5), for the reasons stated beginning on page 2 of the Office Action dated October 20, 2006. The Examiner has asserted that various reference characters in the figures are not mentioned in the description. This objection to the drawings is respectively traversed for the following reasons.

The substitute specification as filed January 9, 2006, has been variously corrected to more clearly describe the reference characters as noted on page 2 of the current Office Action. For example, pages 4-5 of the substitute specification have been corrected to more clearly refer to pre-decode signals PY0_1_2[0:7], PY3_4[0:3], PY5_6[0:3] and PY7_8[0:3], which are described as also referred to in the alternative as PY0, PY1,....PY8 for the sake of brevity. Page 8 of the substitute specification has been corrected to describe that gate signals TGR and TGL are collectively shown as

TGR(L) in Fig. 4, because the pair of signals TGR and TGL provided by a given control block 111 as shown in Fig. 3 have the same values simultaneously responsive to the corresponding block selecting signal YBSEL. With regard to k and l, pages 8 and 9 have been corrected to indicate that [k] and [i], and [l] and [j] are depictions used to characterize respective asserted ones of block selecting signals YBSEL and column selecting signals Y. Also, page 11 has been corrected to describe clock signal CLK as having clock cycle tCYC, as illustrated in Fig. 7.

Applicant respectfully submits that the above noted amendments to the substitute specification follow from the drawings as filed, and thus should not be construed as new matter. Applicant also respectfully submits that the drawings are in compliance with 37 CFR 1.84(p)(5), and thus respectfully urges the Examiner to withdraw this objection.

Specification

The disclosure has been objected to for the various reasons on 3-5 of the current Office Action dated October 20, 2006. This objection is respectfully traversed for the following reasons.

Regarding Fig. 3

As described beginning on page 7, line 11 of the substitute specification, when the input node SBL is the "H" level, the N-channel transistor 55 which is driven by the voltage VDD level generates the voltage drop Vt caused by the threshold voltage. As

subsequently described beginning on page 7, line 17 of the substitute specification, when the input node SBL is the "L" level, the P-channel transistor generates the voltage drop caused by the threshold voltage. Contrary to the Examiner's assertion, voltage drop caused by threshold voltage is described in the substitute specification.

The Examiner has expressed concern regarding how another sense amplifier 301 in another memory cell block 19 can be connected to bit line pair BL[j] and BLb[j] responsive to block selecting signal YBSEL[l] and column selecting signal Y[j], and has also expressed concern regarding the data latching operation. The following comments are offered to help improve the Examiner's understanding of the writing operation, which should be evident for one of ordinary skill in view of the specification as filed.

Fig. 4 illustrates block selecting signal YBSEL[k] and column selecting signal Y[i] which are asserted in a first time period between the first and second vertical dotted lines, and block selecting signal YBSEL[l] and column selecting signal Y[j] which are asserted in a following second time period between the second and third vertical dotted lines. Accordingly, a first memory cell block 19 shown in Fig. 2 is accessed for a writing operation upon assertion of YBSEL[k] (one of YBSEL[0] to YBEL[7] for example) and assertion of Y[i] (one of Y[0] to Y[63] for example) during the first time period. As described in the paragraph beginning on page 8, line 6 of the substitute specification, when YBSEL[k] and Y[i] are high, transistors 222 and 223 of Fig. 3 are on, and data is transferred from data bus DB and DBb to input nodes SBL[i] and SBLb[i] of the sense amplifier 301 of the respective selected memory cell block 19. As further described, at

this time TGR and TGL are low, so that transistors 57, 58, 225 and 226 and transistors 55, 56, 214 and 215 are off, and bit line pair BL[i] and BLb[i] is disconnected from sense amplifier 301.

Then as described beginning in the paragraph on page 8, line 20 of the substitute specification, thereafter during the first time period between the first and second vertical dotted lines, YBSEL[k] changes to low level, causing the TGR signal to go high, so that transistors 57, 58, 225 and 226 in Fig. 3 are turned on, connecting the corresponding sense amplifier 301 of the first accessed memory cell block 19 to bit line pair BL[i] and BLb[i]. As also shown in Fig. 4, during this particular time of the first time period between the first and second vertical dotted lines, Y[i] goes low, whereby transistors 222 and 223 are turned off, to disconnect data bus DB and DBb from sense amplifier 301.

Thereafter, as described beginning on page 9, line 2 of the substitute specification, another block selecting signal YBSEL[l] and corresponding column selecting signal Y[j] are asserted or brought high in the following second time period between the second and third vertical dotted lines shown in Fig. 4. Data is thus transferred from data bus DB and DBb to input nodes SBL[j] and SBLb[j] of another sense amplifier 301 in another respective selected memory cell block 19. During this following second time period, Y[j] turns on transistors 222 and 223 of the another sense amplifier 301, so that data bus DB and DBb are connected to input nodes SBL[j] and SBLb[j] of the another sense amplifier 301. As also shown in Fig. 4, the TGR(L)

signal at this time during the second time period goes low, so that transistors 57, 58, 225 and 226 of the another sense amplifier 301 are turned off, and so that bit line pair BL[j] and BLb[j] are disconnected from the input nodes SBL[j] and SBLb[j] of the another sense amplifier 301.

Accordingly, it should be understood in view of Figs. 2, 3 and 4 taken together, that YBSEL[k] and Y[i] are asserted together during the first time period to conduct a first writing operation from data bus DB and DBb to a first memory cell using a first sense amplifier 301 connectable to bit line pair BL[i] and BLb[i]. It should be further understood that YBSEL[l] and Y[j] are subsequently asserted together during a following second time period to conduct a second writing operation from data bus DB and DBb to a second memory cell using a second sense amplifier 301 connectable to bit line pair BL[j] and BLb[j], and that YBSEL[l] and Y[j] are asserted after YBSEL[k] and Y[i] are no longer asserted.

Regarding Fig. 4

TGR(L), and k and l as used in connection with the YBSEL signals should be understood as explained previously. The paragraph beginning at the bottom of page 4 of the substitute specification explains the interrelationship between the YCLK, CLK, BURST, WDE and DBEQ signals to the extent that would be necessary to provide sufficient understanding for one of ordinary skill. The timing with respect to signals YBSEL, TGR(L), Y[i] and Y[j] and the above noted signals should be clear in view of Fig. 4 and the corresponding description provided in the substitute specification as

emphasized previously. Applicant respectfully submits that it is not clear what further explanation the Examiner would need regarding these signals.

Regarding Fig. 6

It is believed that the concerns regarding Fig. 6 are somewhat similar to those raised with respect to Fig. 3, and that the corresponding discussion given with reference to Fig. 3 should adequately address the Examiner's concerns.

Regarding Fig. 7

As noted previously, the signal tCYC has been described, and should thus be understood. Regarding the TGR(L) signal and the Vpp and VDD levels, the Examiner is respectfully directed to page 10, line 18 through to page 11, line 1; page 11, lines 3-10; page 12, lines 2-7 and page 12, line 23 through to page 13, line 2 of the substitute specification.

Applicant respectfully submits that the specification adequately describes the items noted by the Examiner. The Examiner is therefore respectfully requested to withdraw the objection to the disclosure.

Claim Rejections-35 U.S.C. 112

Claims 1-10 and 12-18 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. This rejection is respectfully traversed for the following reasons.

Regarding claim 1 as addressed by the Examiner, Applicant respectfully submits

that the Examiner has misunderstood operation of sense amplifier block 110 shown in Fig. 3. In the first time period between the first and second vertical dotted lines in Fig. 4, when the YBSEL[k] signal transitions from high to low, NOR gate 53 in a sense amplifier block 110 of the accessed memory cell block 19 outputs signal TGR having a high level. This turns on transistors 57, 58, 225 and 226 of the corresponding sense amplifier block 110, so that bit line pair BL[i] and BLb[i] are connected to the first sense amplifier 301. At this particular time during the first time period, signal Y[i] as shown in Fig. 4 has gone low, so that data bus DB and DBb remain disconnected from sense amplifier 301. Then during the second time period between the second and third vertical dotted lines in Fig. 4, while the status of the first memory cell 19 as noted above is maintained, the YBSEL[l] signal goes high. Accordingly, the output TGR of NOR gate 53, in a sense amplifier block 110 corresponding to the second memory cell 19 to be accessed for a write operation, goes low. Responsive thereto, transistors 57, 58, 225 and 226 of the sense amplifier block 110 corresponding to the second memory cell 19 are turned off, so that bit line pair BL[j] and BLb[j] is disconnected from the sense amplifier 301. At this time, since signal Y[j] is maintained high as shown in Fig. 4, data bus DB and DBb are connected to sense amplifier 301 of the second memory cell 19. Since the status of the sense amplifier block 110 corresponding to the first memory cell 19 to be accessed remains the same as noted above, connection of the second sense amplifier 301 to the data bus DB and DBb occurs during the second time period while bit line pair BL[i] and BLb[i] remain connected to the first sense amplifier 301.

It is important to note that all of signals TGR and TGL over the entirety of memory cell 18 do not simultaneously have the same value as asserted by the Examiner. The values of TGR and TGL change based on which of block selecting signals YBSEL[1] through YBSEL[7] are asserted. Applicant respectively submits that claim 1 is definite and in compliance with 35 USC 112, second paragraph.

Regarding claim 3, when the TGR signal during the second time period between the second and third vertical dotted lines goes from low to high and the Y[j] signal correspondingly goes low, transistors 57, 58, 225 and 226 as shown in Fig. 3 are turned on to connect the second sense amplifier 301 to second bit line pair BL[j] and BLb[j], and transistors 222 and 223 are turned off to disconnect data bus DB and DBb from the second sense amplifier 301.

Claims 4 and 5 should be clear in view of the various previous explanations.

Regarding claim 7, although not necessarily limited thereto, please see the description beginning on page 11 of the substitute specification, wherein the level of array selecting signal XASEL in Fig . 6 controls transistors 84, 85 and 86 to provide either VDD or Vpp as TGR and TGL.

Respective claims 8, 9, 10, 12, 14, 15 and 17 should be clear in view of the various explanations previously given.

With regard to claim 18, although not necessarily limited thereto, please see the description of Fig. 6 in the paragraph beginning at the bottom of page 10 of the substitute specification, wherein the Vpp level is described as a voltage which does not

make a voltage drop between a source electrode and a drain electrode of transistors 214, 215, 225 and 226, and wherein the VDD level is described as a voltage which makes a voltage drop between the source electrode and the drain electrode of the transistors 214, 215, 225 and 226.

Applicant respectfully submits that one of ordinary skill, upon considering the specification taken together with the drawings, would readily understand the scope of the claims as noted above. The Examiner is reminded that the claims should not be considered in a vacuum, but should be considered in light of the specification as would be understood by one of ordinary skill.

Claim Rejections-35 U.S.C. 102

Claims 1-4, 7-9, 12-14, 17 and 18, insofar as understood, have been rejected under 35 U.S.C. 102(b) as being anticipated by the Sakamoto reference (U.S. Patent No. 6,445,632). This rejection is respectfully traversed for the following reasons.

Claim 1 has been amended to include the features of dependent claim 7. The method of storing data of claim 1 includes in combination among other features that "the first bit line is connected to the first sense amplifier via a switching transistor, and wherein the switching transistor is driven to be on by a first voltage and then driven to be on by a second voltage which is higher than the first voltage". Applicant respectfully submits that the Sakamoto reference as relied upon does not disclose these features.

The Examiner has addressed the rejection of claims 1 and 7 together in the

section bridging pages 11 and 12 of the Office Action. However, in this particular section, the Examiner has not establish on the record how the Sakamoto reference may be interpreted as including first and second voltages as features in original claim 7. For the sake of expediting prosecution, claim 1 as amended will be addressed in view of the comments as provided by the Examiner with respect to claim 18 as follows.

The Examiner has asserted with respect to claim 18, and presumably with respect to original dependent claim 7, that bit line isolation control signal ØBIDa as having a low voltage level reads on the first voltage, and that bit line isolation control signal ØBIDa as having a high voltage level reads on the second voltage of the claims. However, as may be understood in view of Figs. 2 and 3 of the Sakamoto reference, when bit line isolation control signal ØBIDa assumes a low level, bit line isolation gate BGDa is disabled so as to isolate bit line pair BLP0 from sense amplifier circuit SAD. Accordingly, bit line isolation gate BGDa in Fig. 2 of the Sakamoto reference as controlled by bit line isolation control signal ØBIDa, is not driven **to be on** by a first voltage, and then driven **to be on** by a second voltage which is higher than the first voltage. Bit line isolation gate BGDa is only driven to be on responsive to a high level of bit line isolation control signal ØBIDa. Applicant therefore respectfully submits that the method of storing data of claim 1 distinguishes over the Sakamoto reference as relied upon, and that this rejection of claims 1-4 is improper for at least these reasons.

For at least somewhat similar reasons, Applicant also respectfully submits that the method of transferring data of claim 18 distinguishes over the Sakamoto reference

as relied upon. That is, responsive to the first voltage, the switching transistor of claim 18 is connected between the sense amplifier and the bit lines so that data having a voltage drop caused by the threshold voltage of the switching transistor **is transferred from the sense amplifier to the bit line** by the switching transistor. On the other hand, responsive to the second voltage which is higher than the first voltage, the data which does not have a voltage drop **is transferred from the sense amplifier to the bit line**. Clearly, when bit line isolation control signal ØBIDa in Fig. 2 of the Sakamoto reference assumes a low level, bit line isolation gate BGDa is turned off and **does not transfer data** from sense amplifier SAD to bit line pair BLP0. Bit line isolation control signal ØBIDa therefore cannot be interpreted as providing first and second voltages to a switching transistor, as would be necessary to meet the features of claim 18. Applicant therefore respectfully submits that the method of transferring data of claim 18 distinguishes over the Sakamoto reference as relied upon, and that this rejection is improper for at least these reasons.

With further regard to this rejection, claim 8 is directed to a method of **storing data**, and includes in combination among other features transferring first data **from** a data line **to** a first sense amplifier when a first bit line is disconnected from the first sense amplifier.

In contrast, the Sakamoto reference as specifically relied on by the Examiner is directed to **reading data from a memory cell**. For instance, as described in column 6, lines 39-41 of the Sakamoto reference, when a row or word line is designated in

memory block 1a of Fig. 1, one of sense amplifier bands 2u and 2d senses, amplifies and latches data of (from) the memory cells in the selected row. As further described beginning in column 8, line 65 of the Sakamoto reference, when word line WL0 in Fig. 2 of the Sakamoto reference is driven into the selected state by row selection circuitry, data of memory cells MC connected to word line WL0 **are read onto** the corresponding bit line pairs BLP0 and BLP1, and then transmitted to sense nodes of sense amplifier circuits SAU through bit line isolation circuit 3ua. As further described in column 9, lines 10-13 of the Sakamoto reference, memory cell data which has been transmitted to the sense nodes of the sense amplifier circuit SAU is amplified and latched by sense amplifier circuit SAU. As further described beginning in column 9, line 25 of the Sakamoto reference, a read command READU instructs data reading.

The Examiner has interpreted internal data line pair IOP in Fig. 2 of the Sakamoto reference as the data line of claim 8. However, as should be understood particularly in view of the above noted portions of the Sakamoto reference, the circuit in Fig. 2 of the Sakamoto reference does not transfer data **from** internal data line pair IOP **to** sense amplifier SAU, as would be necessary to meet the features of claim 8. In contrast, in the Sakamoto reference as relied on, data is read **from** memory cell MC via bit line pair BLP0 for example, **to** sense amplifier SAU, to be subsequently output via internal data line pair IOP shown in Fig. 2. The Sakamoto reference as relied upon does not specifically disclose or suggest storing data in memory as would be necessary to meet the features of claim 8. Applicant therefore respectfully submits that the

method of storing data of claim 8 distinguishes over the Sakamoto reference as relied upon, and that this rejection of claims 8, 9 and 12 is improper for at least these reasons.

The method of storing data of claim 13 includes in combination among other features "transferring first data from a data line to a first sense amplifier, wherein the first data is latched in the first sense amplifier". Applicant respectfully submits that the Sakamoto reference as specifically relied upon does not disclose a method of storing data, but in contrast specifically discloses reading data from memory. Applicant therefore respectfully submits that the method of storing data of claim 13 distinguishes over the Sakamoto reference as relied upon, and that this rejection of claims 13, 14 and 17 is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 5, 6, 10, 11, 15 and 16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Sakamoto reference in view of the Kwon et al. reference (U.S. Patent No. 5,973,972). Applicant respectfully submits that the Kwon et al. reference as secondarily relied upon does not overcome the above noted deficiencies of the Sakamoto reference, and that this rejection of claims 5, 6, 10, 11, 15 and 16 is therefore improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding objections and rejections, and to pass the claims of the present application to issue, for at least the above reasons.

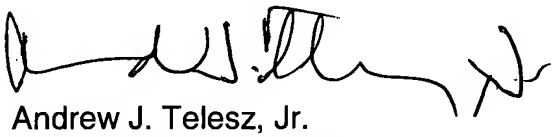
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of two (2) months to March 20, 2007, for the period in which to file a response to the outstanding Office Action. The required fee of $450.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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